



Model 560-5170-1
4.1978 Hz FREQUENCY SYNTHESIZER

SECTION ONE

1. FUNCTIONAL DESCRIPTION
 - 1.1. PURPOSE OF EQUIPMENT
 - 1.2. PHYSICAL SPECIFICATIONS
 - 1.3. ENVIRONMENTAL SPECIFICATIONS
 - 1.4. POWER REQUIREMENTS
 - 1.5. FUNCTIONAL SPECIFICATIONS
 - 1.5.1. REF A, B, AND C INPUTS
 - 1.5.2. TTL OUTPUTS
 - 1.5.3. RS-422 OUTPUTS
 - 1.5.4. OUTPUT FREQUENCY
 - 1.5.5. CARD COMPATIBILITY

SECTION TWO

2. INSTALLATION AND OPERATION
 - 2.1. HOT SWAPPING
 - 2.2. REMOVAL AND INSTALLATION
 - 2.3. SETUP
 - 2.3.1. PASSIVE COMBINER SELECT SWITCHES
 - 2.3.2. INPUT FREQUENCY SELECT SWITCH
 - 2.3.3. OUTPUT DRIVE SELECT SWITCH
 - 2.3.4. CPU / LOCAL MODE SELECT SWITCH
 - 2.3.5. LOCAL MODE FREQUENCY SELECTION SWITCHES
 - 2.3.6. PRIMARY SYNCHRONIZATION INPUT SWITCH
 - 2.3.7. SECONDARY SYNCHRONIZATION INPUT SWITCH
 - 2.3.8. PRIMARY SYNCHRONIZATION ENABLE SWITCH
 - 2.3.9. SECONDARY SYNCHRONIZATION ENABLE SWITCH
 - 2.3.10. DELAY SWITCH
 - 2.4. CPU MODE FREQUENCY SELECTION
 - 2.5. FAULT INDICATIONS
 - 2.5.1. SYNTH. FAULT
 - 2.5.2. OUT FAULT
 - 2.5.3. INIT. FAULT
 - 2.5.4. DETAILED FAULT STATUS VIA CPU

SECTION THREE

3. THEORY OF OPERATION
 - 3.1. GENERAL INFORMATION
 - 3.2. HARDWARE DESCRIPTION
 - 3.3. DETAILED DESCRIPTION
 - 3.3.1. PASSIVE COMBINER
 - 3.3.2. POWER SUPPLY
 - 3.3.3. VOLTAGE CONTROLLED OSCILLATOR
 - 3.3.4. FPGA / DDS
 - 3.3.5. FILTERS / COMPARATORS
 - 3.3.6. OUTPUT DRIVERS
 - 3.3.7. FAULT DETECTION
 - 3.3.8. BACKPLANE FAULT OUTPUT

3.3.9. FAULT INDICATORS

SECTION FOUR

4. DETAILED DRAWINGS
 - 4.1. 560-5170-1 DETAILED DRAWINGS / BILL OF MATERIALS

SECTION ONE

1 FUNCTIONAL DESCRIPTION

1.1 PURPOSE OF EQUIPMENT

The TrueTime 560-5170-1 Frequency Synthesizer is a special plug-in option card for the Model 56000 DRC. In a system that includes a Fault Monitor/CPU card, this option card offers the unique frequency of 4.1979 hertz.

The Frequency Synthesizer generates an output frequency that is locked to the external reference frequency distributed via REF A, B, or C on the backplane. The input frequency from the REF A, B, and C inputs (1, 5, or 10 MHz) is switch-selectable by an on-card DIP switch. The reference is received via the passive combiner, which passes only the currently-highest priority reference to the synthesizer. If the currently-highest priority reference is changed, the passive combiner shifts to the next-highest priority input and the synthesizer locks to the new reference.

In a system without a Fault Monitor CPU card, the Frequency Synthesizer card offers automatic REF A, B, C passive combiner operation as previously stated. When the synthesizer card is used in a system that includes the Fault Monitor CPU card, the REF A, B, C inputs are also controlled by the CPU. When a REF A source's Fault Status is detected (monitored by the CPU), the REF A input on the synthesizer card is disabled. The REF B and REF C inputs are operated similarly -- they are turned off whenever a Fault Status condition for that reference exists. The CPU's REF A, B, C control feature ensures that only a viable reference oscillator is used on the 560-5170-1 card.

The 4.1978 Hz frequency is supplied to the backplane as a common bused signal and driver/buffer cards drive the output to the backplane connector via six complementary drivers. The output signals are delivered to external cables via the I/O card installed in the rear slot directly behind the driver cards. Output drive capability is switch-selectable for RS-422 / 100 ohm or TTL / 50 ohm. NOTE: The TTL setting provides enhanced drive capability, but allows the short circuit current to exceed the RS-422 specification. The output mode, single-ended or differential, is determined by the type of I/O card that is installed.

1.2 PHYSICAL SPECIFICATIONS

Dimensions: 0.8"w X 3.94"h X 8.66"d (2 cm X 10 cm X 22 cm)
Weight: Approximately ½ pound (¼ kg)

1.3 ENVIRONMENTAL SPECIFICATIONS

Operating Temp: 0° to +50°C
Storage Temp: -40° to +85°C
Humidity: Up to 95% relative, non-condensing

Cooling Mode: Convection
Altitude: Sea Level to 10,000 ft.

1.4 POWER REQUIREMENTS

Voltage: 18-72 VDC
Power: 7 W (outputs A through F driving 50 Ω)

1.5 FUNCTIONAL SPECIFICATIONS

1.5.1 REF A, B, and C INPUTS

Signal Type: Squarewave or Sinewave
Amplitude: 2-5 Vpp
Frequency: 1, 5, or 10 MHz (switch-selectable)

1.5.2 TTL OUTPUTS (SW2-4 = ON)

Quantity: 6
Signal Type: Squarewave, TTL-level
Amplitude: 2.8 Vpk into 50 ohms

1.5.3 RS-422 OUTPUTS (SW2-4 = OFF)

Quantity: 6
Signal Type: Squarewave, centered at 2.5 VDC
Amplitude: 2.8 Vpp into 100 ohms
Output Drive: MIL-STD-188-114A TYPE II
Compliance: BALANCED RS-422-A

1.5.4 OUTPUT FREQUENCY

Frequencie: 4.1978 Hertz

Frequency Stability:

Long-term: Equal to reference on REF A, B, or C

Short-term: Better than 1 part in 10^9 (1 second average)

Timing: Rising Edge < 500 ns output to output

Phase noise: -50 dBc/ $\sqrt{\text{Hz}}$ @ 4 Hz from carrier

Spurious: -60 dBc

1.5.5 CARD COMPATIBILITY

Location: Slot 1-17 with compatible I/O card in rear slot.

Compatibility: See Card Compatibility Matrix.

SECTION TWO

2 INSTALLATION AND OPERATION

2.1 HOT SWAPPING

All cards, input cables, and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. Hot swapping and reference-source changes are abrupt, the effects difficult to characterize; however, the system is designed to protect against permanent effects and minimize temporary effects of these events. Typically, adjacent-card hot swapping has a negligible effect on the Frequency Synthesizer. Although the hot swapping event directly affects the control voltage of each on-board oscillator, it typically lasts less than one clock-period and has an average of 0 Volts. The effect of redundant power supply switch-over is also negligible.

The effect of a reference-source change is less predictable. The reference frequency is delivered via REF A, B, and C on the backplane. The Frequency Synthesizer receives the reference via the Passive Combiner. If the currently-highest priority reference is changed, the Synthesizer locks to the new reference. When the new reference is in phase with the old reference, the output frequency is affected by less than 1 part in 10^8 over a 1 second period. When the new reference is of opposite phase, the effect can approach 1 part in 10^6 . The frequency-shift occurs relatively softly over a 100 ms period, minimizing any effect on downstream equipment. Note that hot swapping a local frequency source, such as an oscillator or fiber optic receiver, qualifies as a hot swap and reference-source change.

The effect of a reference-input perturbation that does not result in a reference-source change (e.g. - removing a cable that is not currently-highest priority) at the passive combiner also has an effect on the Frequency Synthesizer. This is due to the fact that the reference frequency used by the synthesizer is always a weighted sum of REF A, B, and C, and any change has some effect on the resultant waveform. The effect is usually negligible, but can approach 1 part in 10^8 .

2.2 REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle (or on any connector on rear panel adapter cards) at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced.

Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3 SETUP

The setup of the 560-5170-1 Frequency Synthesizer card involves setting the following DIP switches:

Required switch settings:

1. Passive Combiner Select Switches (SW6 - SW10)
2. Input Frequency Select Switch **Fixed N/A** (SW2-2 & SW2-3)
3. Output Drive Select Switch Disabled (SW2-4)
4. CPU / LOCAL Mode Select (SW1-4)
5. Output Frequency Selection Switches **Fixed N/A** (SW3 & SW2-1)
(used only in local mode)

6 thru 10 not available (synchronous or phase alignment)

6. Primary Synch Input Switch (SW12)
7. Secondary Synch Input Switch (SW11)
8. Primary Synch Input Enable Switch (SW4)
9. Secondary Synch Input Enable Switch (SW5)
10. Delay Switch (activity time-out) (SW1-1 through SW1-3)

2.3.1 PASSIVE COMBINER SELECT SWITCHES (SW6 through SW10)

SW6 through SW10 MUST be set to match the REF A, B, and C input frequency.

PASSIVE COMBINER	10 MHz	5 MHz	1 MHz
SW6-1 THRU SW10-1	ON	OFF	OFF
SW6-2 THRU SW10-2	OFF	ON	OFF
SW6-3 THRU SW10-3	OFF	OFF	ON
SW6-4 THRU SW10-4	OFF	OFF	OFF

2.3.2 INPUT FREQUENCY SELECT SWITCH (SW2-2 & SW2-3)

This switch sets the internal divider for the PLL control. This switch MUST be set to match the input frequency in use -- REF A, B, and C.

INPUT FREQUENCY SELECT	SW2-2	SW2-3
1 MHz	OFF	OFF
5 MHz	OFF	ON
10 MHz	ON	OFF

2.3.3 OUTPUT DRIVE SELECT SWITCH (SW2-4)

Not Available Set SW2-4 to select the output drive mode:

SW2-4	ON: TTL / 50 ohms
SW2-4	OFF: RS-422 / 100 ohms

2.3.4 CPU / LOCAL MODE SELECT SWITCH (SW1-4)

SW1-4 is the CPU / LOCAL select switch. If the switch is ON, the card will be operated in LOCAL mode which uses the nine on-board frequency setting switches to select one frequency rate for all six outputs. If the switch is OFF, the card will be operated in CPU mode which allows independent serial port control on each of the six outputs.

SW1-4 CPU Mode	OFF
SW1-4 LOCAL Mode	ON

2.3.5 LOCAL MODE FREQUENCY SELECTION SWITCHES (SW3 & SW2-1) NOT AVAILABLE

Frequency is fixed at 4.1978 Hertz.

2.4 THIS SECTION NOT USED

2.5 FAULT INDICATIONS

All indicators activate briefly following hot-insertion or power-up. The following paragraphs describe operation during steady-state conditions.

2.5.1 SYNTH. FAULT

The Synthesizer Fault indicator may flash briefly during hot swapping and at the addition or removal of REF A, B, or C. This is a normal condition which occurs as the Voltage Controlled Oscillator (VCO) experiences a reference perturbation (see HOT SWAPPING section for a discussion of the effects of hot swapping).

A continuously-flashing indication shows either a phase-locked loop out-of-lock condition or, when enabled, the loss of both Primary and Secondary input synchronization inputs. A solid ON SYNTH FAULT LED indicates a local power supply failure.

Loss-of-lock (blinking SYNTH FAULT LED) could be caused by:

- 1) Input reference off-frequency.
- 2) Loss of reference on REF A, B, and C. When all references are lost, the VCO drifts to one end of the control range, which is detected as a SYNTH FAULT.
- 3) A VCO Failure.

2.5.2 OUT. FAULT

The OUT A through OUT F Fault indicators activate when the associated driver has failed. When the card is in the RS-422 output mode, a failure of either the +Output or -Output will activate the indicator, whether or not both outputs are available at the rear I/O Card connector. When the card is in the TTL output mode, only the OUT A through F outputs are fault detected. Note that the detector is designed to detect failed drivers and, typically, will not detect a shorted output.

2.5.3 INIT. FAULT

This is an on-card fault indicator which is not externally visible; although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Activation of this LED is accompanied by activation of all of the front panel indicators. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a power or hot swap cycle. If this is unsuccessful, the card is defective.

2.5.4 DETAILED FAULT STATUS VIA CPU

The Fault Monitor CPU has access to detailed 560-5209 card status. This status is available via the Fault Monitor CPU serial port. When it is presented in a 2-byte format, with individual bit definitions as follows:

The Verbose report displays the Fault status. In this context, a reported fault indicates a problem. The Machine report, when used, reports the current status (settings) of the switches and faults in hexadecimal characters. Together, they pinpoint problems and help the technician view the switch settings on the cards without removing them.

2.5.5 VERBOSE REPORTS

The following is an example of a Fault Monitor CPU report in Verbose mode:

```
TrueTime 56000 Site 01
Automatic Reports Enabled
Periodic Reports Disabled
Primary Inputs Selected REFA No REFB No REFC Off PRI OK SEC OK TER Off

1. Undefined      OK          Undefined      OK
2. Undefined      OK          Undefined      OK
3. 5170-1 LOCAL OSC FAULT 0407 Undefined OK
4. Undefined      OK          Undefined      OK
```

The above sample tells you that:
Automatic reports are enabled and Periodic reports are disabled.

Primary inputs REF A and REF B are not bussing AUX REF. REF C is off. Primary and Secondary status inputs OK, Tertiary is OFF.

Numbers 1-4 are slots (not all slots are shown in the example). Slots 1,2,and 4 are undefined (empty) and functional (OK).

Slot 3 is read as follows:
5170-1 is the abbreviation of the 560-5170-1 card. The fault reading is 0407.

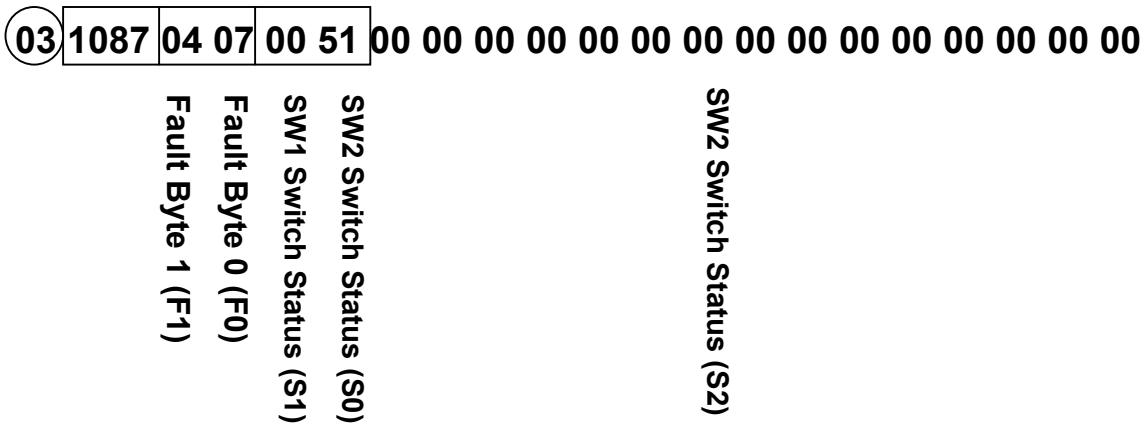
2.5.6 MACHINE REPORTS

The Fault Monitor CPU has another serial output mode called machine report mode. This mode is usually used with a computer program to interrogate the 56000 system status. The machine report mode displays hexadecimal (HEX) characters like the verbose mode report.

The following is an example of a Fault Monitor CPU report in Machine Mode:

```
TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 10 87 04 07 0051 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)
```

Example from card slot 3 above:



Slot 3 shows that the Fault status is 0407 (F1, F0). The Status report read-out is 0051(S2,S1,S0).

2.5.7 REPORT CONVERSIONS

This section deals with how to read and convert the Fault and Status read-outs using various tables and binary conversions. To decipher a Fault Status report, use Fig. A. For Status reports (S2, S1, S0) use Fig. B.

Fig. A

Spare	Spare	Spare	Spare	Primary Source	Sec. Input Inactive*	Pri. Input Inactive*	Power Cycled	Undefined	Synthesizer*	Output Fault E	Output Fault D	Output Fault C	Output Fault B	Output Fault A	Output Fault F
8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1
Upper Byte High Nibble 0				Upper Byte Low Nibble 4				Lower Byte High Nibble 0				Lower Byte Low Nibble 7			
Fault Status F1 Report								Fault Status F0 Report							
Key:															

Above each 8,4,2,1 is the corresponding fault for that bit. For instance, above the 8 bit in the Upper byte/Low nibble reads Rub. Lockmon, which is the fault .

Shaded area

Informational only. The upper row: Bit value hex weights (8,4,2,1) The Lower row corresponds to the hex weight above. For instance, 2^3 is 8 in binary.

Each section of 8,4,2,1 is a nibble of either an Upper or Lower byte and separated for easy recognition. Each nibble = 4 bits and each byte = 8 bits. "04" is the F1 report, "07" the F0 report.

Non-shaded area

This area is used according with the report read-out after a report is converted to binary. The 0407 is an example from a report.

Always read the report from Upper (High) byte to Lower (Low) Byte.

** Bit set when bit errors are detected in IRIG-B.

*** These controls are not implemented at this time.

* Latched Fault Bit -- Reset Via Fault Monitor CPU.

Always read the report from Upper (High) byte to Lower (Low) Byte.

Status (S2, S1, S0) Conversion Table

FIG. B

STATUS REG 0	Bit	Bit Value	Switch	
Low	0	1	Pri Input Enable SW4-1	1
Nibble	1	2	Pri Input Enable SW4-2	
Low	2	4	Pri Input Enable SW4-3	
Byte	3	8	Pri Input Enable SW4-4	
High	4	1	Sec Input Enable SW5-1	5
Nibble	5	2	Sec Input Enable SW5-2	
Low	6	4	Sec Input Enable SW5-3	
Byte	7	8	Sec Input Enable SW5-4	
STATUS REG 1				
Low	0	1	Freq Set Switch SW3-1	0
Nibble	1	2	Freq Set Switch SW3-2	
High	2	4	Freq Set Switch SW3-3	
Byte	3	8	Freq Set Switch SW3-4	
High	4	1	Freq Set Switch SW3-5	0
Nibble	5	2	Freq Set Switch SW3-6	
High	6	4	Freq Set Switch SW3-7	
Byte	7	8	Freq Set Switch SW3-8	
STATUS REG 2				
Low	0	1	Freq Set Switch SW2-1	2
Nibble	1	2	Input Freq Select Switch SW2-2	
Low	2	4	Input Freq Select Switch SW2-3	
Byte	3	8	TTL Mode SW2-4	
High	4	1	Delay timeout SW1-1	0
Nibble	5	2	Delay timeout SW1-2	
High	6	4	Delay timeout SW1-3	
Byte	7	8	Always 0	

Notes: The settings listed under the Switch column are HIGH or ON. For instance, frequency has SW 1-1 and SW 1-2. If SW 1-1 is ON, SW 1-2 is presumed to be OFF (although there is no specific mention of this). For switches, a 1 = ON, 0 = OFF.

* Latched Fault Bit—Reset Via Fault Monitor CPU

Graphically, the switch settings look like this:

Switch/Position	10 MHz	5 MHz	1 MHz
1 1	1 (On)	0 (Off)	1 (On)
1 2	0 (On)	1 (On)	1 (On)

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:

1 = Fault/Switch On
0 = No Fault/Switch Off

Use the Binary Conversion table to convert a read-out from the monitor to binary. For instance, if the report read-out was 3C15, this would be:

11\1100\1\101 in binary.

USING THE FAULT STATUS REPORT (F0, F1)

The hex weight (fault importance) has been assigned 8, 4, 2, 1. Beneath each number is the corresponding fault. Use Fig. A. The report example read 0407. The 0 is high byte/high nibble, the 4, high byte/low nibble, the 0, low byte/high nibble and 7, low byte/low nibble. Each nibble falls under a section on Fig. A, high to low or left to right.

Look at Fig. A.. Below this is a sample read-out. This read-out would appear on the monitor when a Verbose report is requested. In the example, there are no faults in the upper byte/high nibble or in the lower byte/high nibble because both are zero (0). In the upper byte/low nibble, a 4 is reported. Looking directly above this, a 4 bit is easily spotted. The fault is Secondary Input Inactive. However, In the lower byte/low nibble a 7 is reported. There is no 7 listed, only a 1, 2, 4, 8. Use the Binary Conversion table to determine the faults.

Seven (7) is converted to 111 in Binary. In Binary, a 1 = fault and 0 = no fault. Read 111 from right (low bit) to left (high bit) using the lower byte/low nibble group. The first three (from low bit to high bit) are 1's, indicating there is a fault with the Output Faults F, A and B.

Note that the hex weight assigned totals to 7 (4+2+1). If the 7 had been a 6, in binary this is 110. Reading from low bit to high bit, the 1's (i.e., faults) fall under hex weight 4 and 2, which equals a hex weight of 6. Of course, glancing at the lower byte/low nibble, you can quickly see (without converting to binary) that under 4 and 2 (i.e., 6) are the Output B and Output A that are in fault.

Each of the four nibbles is grouped by category for easy visual identification of an offending fault. Each nibble has 15 possible fault combinations. All faults are asserted as a logic 1. The faults are latched on the Oscillator card and must be cleared by the 560-5179-1 Fault Monitor CPU "CL" command.

USING THE STATUS REPORT (S2, S1, S0)

The method used for reading the Fault report is the same when reading the Status report. Refer to Fig. B.

Using the read-out, 0051, but because the table is different, the 0 is located at the high nibble/high byte of S1. The rest of the numbers follow upward towards the low byte and ending in Status 0. In this case, the 0 falls in the high nibble/high byte section of S1

1 = Active, 0 = Not active.

Since we have a 5 in the high nibble/low byte(from top to bottom) in Status 0. The readout of 5 must be converted to 101 in binary. The 101 is inserted in the section from low bit to high bit (in the high nibble/low byte section of Status 0).

Sec Input Enable SW5-1	1
Sec Input Enable SW5-2	0
Sec Input Enable SW5-3	1
Sec Input Enable SW5-4	0

Now we see that SW5-1 and SW5-3 are active.

In the Status Register 2 section, the 2 is in the low nibble/low byte section indicating that the Input Freq Select Switch SW2-2 is active.

QUICK REFERENCE SHEET FOR READING FAULT AND STATUS REPORTS

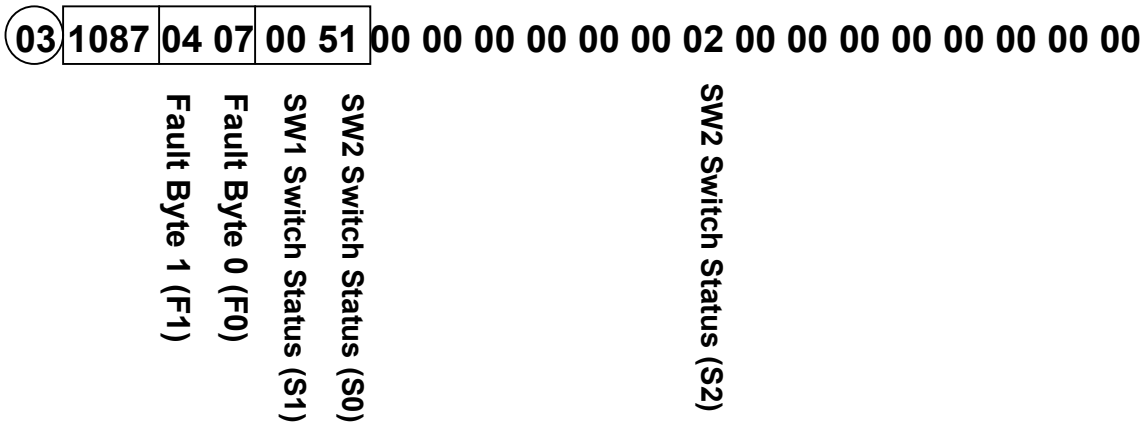
1. Run a report. This is a portion of a sample Machine report.

```

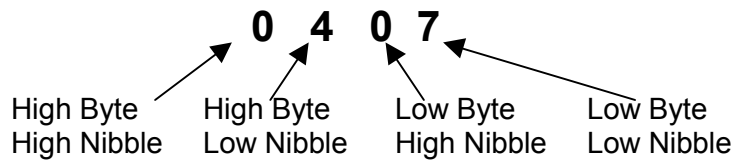
TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 10 87 04 07 00 51 00 00 00 00 00 00 00 02 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)
    
```

0407 is the Fault Status read-out
 0051 is the Status read-out report

04 = Fault Status 1 (F1) report
 07 = Fault Status 0 (F0) report
 00 = Status 1 (S1) report
 51 = Status 0 (S0) report



What's in a number?



2. When required, convert Decimal to Binary using the Binary Conversion Table.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:

1 = Fault/On/Active

0 = No Fault/Off/Not Active

SECTION THREE

3 THEORY OF OPERATION

3.1 GENERAL INFORMATION

This section contains a detailed description of the circuits used on the N8 Frequency Synthesizer card. Use these descriptions in conjunction with the drawings in SECTION FOUR.

3.2 HARDWARE DESCRIPTION

The 4.1978 Hz Frequency Synthesizer incorporates a Passive Combiner, a DC-to-DC Converter, a phase-locked VCO, six DDS (Direct Digital Synthesis) ICs to generate the six output frequency rates, 12 Output Drivers (six differential pairs), Fault-detection circuitry and 7 Fault Indicators.

3.3 DETAILED DESCRIPTION

Reference drawing 560-5170-1.

3.3.1 PASSIVE COMBINER (Sheet 8)

The passive combiner is a circuit that strives to always output the desired signal, derived from the three separate inputs REF A, B, and C. The passive combiner minimizes any switching transient or glitch when one or two of the inputs are lost. It is composed of three input filter sections, three high speed comparators, a weighting network and a passive combining network. The filters and the combining network employ tuned circuits and therefore have to have their values adjusted depending on the required input frequency of either 1, 5, or 10 MHz. This is accomplished by the use of SW6 through SW10, which are 4PST DIP switches. The input filters and the comparators serve to produce a very clean square wave with very good symmetry. These square waves are then buffered and applied to the weighting network where they are summed with different weights in order to give the primary source the greatest influence on the final result. This summing results from an interaction between the weighting network and the combining network which is composed of a parallel resonant tank and a series resonant tank. These tanks are tuned slightly off center, lowering the Q, so that amplitude variations are minimized when input signals are changed. The final output voltage is then buffered and squared to produce the final signal called FREQIN.

3.3.2 POWER SUPPLY (Sheet 10)

The DC-to-DC Converter converts 48 VDC backplane power to local ± 5 VDC power. It is fully-isolated from the backplane power and referenced to signal GND on the N8 Synthesizer card. Backplane power is supplied via a Polyswitch fuse device, diode

and Pi-section L-C filter. The poly-fuse protects the backplane power bus from internal DC-to-DC shorts. The diode and L-C filter serve a triple purpose. During live insertion, the high-current inductor minimizes in-rush current to the DC-to-DC being inserted; and, the diode and capacitor serve to hold up the local voltage at the input to each currently-installed DC-to-DC. During steady-state conditions, the L-C filter minimizes switching noise coupled back into the backplane power bus. During live-extraction, the 0.1 uF capacitor absorbs the inductive-kick of the opened circuit, minimizing contact-arcing. The -5 VDC side of the supply is artificially loaded, providing a minimum load to improve output voltage regulation. The power-up reset generator, assures that RESET is active while the +5 VDC supply is between 1 and 4.5 VDC. This guarantees proper configuration of the Xilinx FPGA during hot swapping and power-up.

3.3.3 VOLTAGE CONTROLLED OSCILLATOR (Sheet 7)

The card is equipped with a 32.768 MHz VCO. This VCO is phase locked to a 1 MHz reference frequency that is derived from REF A, B, and C inputs (FREQIN). The FPGA provides a divider and phase-comparator for the FREQIN signal and the 32.768 MHz on-board oscillator. The filtered phase comparison output from the loop filter integrator connects to the voltage control input on the 32.768 MHz oscillator; closing the loop. The 32.768 MHz output is the clock source for the six DDS frequency synthesizer ICs.

3.3.4 FPGA / DDS (Sheets 4, 5, & 6)

FPGA U4 provides the timing and control signals for the N8 synthesizer in both LOCAL and CPU modes. When the N8 is operated in LOCAL mode, frequency select switches SW3 and SW2-1 are used to program the six synthesizer ICs with the same output frequency rate. After the FPGA sets the frequency registers in all six DDS ICs, all six DDS ICs are synchronized to the Primary or Secondary synchronization input (if this function is enabled). This synchronization input allows the N8 frequency rates to not only be frequency locked but to also be phase synchronized to the other outputs in the system.

In a system that includes a Fault Monitor/CPU assembly, the FPGA is the interface between the Frequency Synthesizer and the CPU. When the synthesizer card is operated in the CPU mode, the Fault Monitor/CPU assembly monitors the fault status only. No frequency setting is available via the CPU as the synthesizer card is at a fixed frequency.

3.3.5 FILTERS / COMPARATORS (Sheet 6)

The differential sine wave outputs from each DDS IC are connected through an LC filter to a voltage comparator. The voltage comparators convert the differential sine waves to single-ended outputs.

3.3.6 OUTPUT DRIVERS (See the 560-5181-2 driver card manual.)

3.3.7 FAULT DETECTION (Sheets 4, 7 & 9)

There are three categories of fault detection: Input, Output and PLL faults. All three fault detector categories use a combination of discrete components and Xilinx FPGA logic to perform the detection task.

Primary and Secondary, are detected for voltage levels using voltage comparators. The synchronization signals are then qualified for activity (if enabled) by the FPGA. Watchdog timers inside the FPGA compare the synchronization signals to the Delay switch time-out setting. If both Primary and Secondary synchronization input sources are deemed bad, the FPGA communicates this condition to the SYNTH FAULT LED and to the CPU card (if installed).

The output driver fault detector consists of two 1 of 8 analog multiplexers that sample 12 outputs in RS-422 mode or 6 outputs in TTL mode. The multiplexers are under control of the FPGA. The multiplexers sample each of the outputs and pass the sampled output to a mono-stable that is used as a watchdog timer. If the sampled output is not switching (bad), the output from the watchdog timer will provide a logic high to the FPGA which recognizes this as an output signal fault. Logic inside the FPGA continually verifies the condition of each output. Failure to detect a signal from an output results in activation of the appropriate OUT fault indicator and reports the failure to the CPU card (if installed).

The Frequency Synthesizer (SYNTH FAULT) detector utilizes four voltage comparators to detect an out-of-lock condition in the 32.768 MHz VCO. These comparators verify that the VCO control voltage and filtered phase comparator voltage are within defined limits. If the control voltage is out of tolerance, circuitry in the FPGA is activated and communicates this condition to the SYNTH FAULT LED and to the CPU card (if installed).

3.3.8 BACKPLANE FAULT OUTPUT

Inside the FPGA, all faults are combined to form a composite fault signal which is used to drive the Fault line to the Fault Monitor CPU. Fault-signal active indicates status-bit true. (Note that FAULT signal is active low on the backplane.) Refer to manual section 2.5.4 for detailed information on the fault reporting.

3.3.9 FAULT INDICATORS (Sheet 10)

The INIT. FAULT indicator is driven by the FPGA Initialization-done signal. It activates during initialization, and remains active if initialization does not complete. This is an extremely unusual occurrence.

The SYNTH. FAULT indicator is powered directly from the backplane 48 VDC power buss and is controlled via an opto-isolator to maintain 48 VDC isolation. If local 5 VDC power is lost, the SYNTH. FAULT indicator will be ON solid.

3.3.9.1 SYNCHRONIZATION INPUT FAULT

The SYNTH. FAULT indicator is not turned ON from this fault source if either the Primary or Secondary synchronization inputs are viable or if the synchronization function is disabled. If both the Primary and Secondary inputs are lost and the function is enabled, the SYNTH. FAULT indicator will blink ON and OFF.

3.3.9.2 PLL FAULT

The SYNTH. FAULT indicator is not turned ON from this fault source when the 32.768 MHz VCO is locked and functioning within limits. When the 32.768 MHz VCO is not locked, the SYNTH. FAULT indicator will blink ON and OFF.

3.3.9.3 OUT FAULT

The OUT fault indicators are controlled directly by the fault detection logic. NOTE: In RS-422 mode, OUT A through F LEDs indicate when either a non-complimented or complimented output fault condition exists.

SECTION FOUR

4 DETAILED DRAWINGS

4.1 560-5170-1 DETAILED DRAWINGS / BILL OF MATERIALS